UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/601,617	06/23/2003	Louis A. Lippincott	42P17012	8912

8791 7590 12/20/2005

BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES, CA 90025-1030

EXAMINER	
TUNG, KEE M	

ART UNIT	PAPER NUMBER
2671	

DATE MAILED: 12/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/601,617	LIPPINCOTT ET AL.	
	Examiner	Art Unit	
	Kee M. Tung	2671	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The response filed 10/17/05 has been considered in preparing this Office action.

Claim Rejections - 35 USC § 112

1. Claim 6 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claim 6, line 2, "may be" is indefinite for fails to recite positive claimed language.

2. Claim 28 (old 29) recites the limitation "the SDRAM" in line 1. There is insufficient antecedent basis for this limitation in the claim. Changing the claim dependency from claim 21 to claim 27 (old 28) would over come the rejection.

3. The numbering of claims is not in accordance with 37 CFR 1.126 which requires the original numbering of the claims to be preserved throughout the prosecution. When claims are canceled, the remaining claims must not be renumbered. When new claims are presented, they must be numbered consecutively beginning with the number next following the highest numbered claims previously presented (whether entered or not).

Misnumbered claims 28 and 29 have been renumbered to claims 27 and 28.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-28 (original filed claims 1-26, 28 and 29, there is no claim 27) are rejected under 35 U.S.C. 103(a) as being unpatentable over Lewis (GB 2, 386,442) in view of Potts (US 6,477,177).

Lewis teaches a processor (Fig. 1, data processing system 10) comprising a plurality of processing elements (DSP1 and DSP 2); and a plurality of hardware accelerators (Accelerators 11a-11c) coupled to a selection unit (13). However, Lewis fails to explicitly teach or suggest a register file coupled to the selection unit and the plurality of processing elements, the register file including a plurality of general purpose registers accessible by the plurality of hardware accelerators, the selection unit and the plurality of processing elements, at lest one of the general purpose registers including at least one bit to allow a processing element to direct the selection unit to activate a selected hardware accelerator. This is what Potts teaches (Fig. 2). Potts teaches a plurality of processors (120 and 122) access to the plurality of time slot registers (Fig. 2, 210-222) and a configuration control register (220) to contain suitable bit setting to allow the processors to access one of the plurality of registers (abstract). It would have been obvious to one of ordinary skill in the art at the time the present invention was made to combine the teachings of register file of Potts into the system of Lewis in order to allow the plurality of processing element to better and more efficiently share access to one of the plurality of resources (such as, hardware accelerators or time slot registers) as taught by Potts (col. 6, lines 37-45) and further to assist in maximizing the efficiency of processors and hence assist in the reduction of power consumption, silicon size as well

as cost as taught by Lewis (page 9, 10-12). Therefore, at least claim 11 would have been obvious.

Method claim 1 and an article of manufacture claim 6 recited similar features as claim 11, and thus are rejected under similar rationale.

As per claim 21, the combined system further teaches a memory interface (inherent by the teaching of memory bus of Lewis, page 1, line 4 of third paragraph) coupled to one or more of the media processors; and a RAM coupled to the memory interface (inherent that the memory bus is coupled to a memory device). However, the combined system fails to explicitly teach or suggest a plurality of media signal processors. It would have been obvious to one of ordinary skill in the art at the time the present invention was made to implement the teachings of the combined system of Lewis and Potts because multiple or plural processors provide better and much faster system performance as well known in the art and further to add or subtract a number of processors into the system is considered within the level of ordinary skill in the art (see similar example of change number of the DSP and accelerators as taught by Lewis, page 4, lines 5-6 and 10-11). Therefore, at least claim 21 would have been obvious.

As per claim 2, the combined system further teaches enabling a processing element to set a bit when the process desires selection of a hardware accelerator (Lewis, paragraph bridge at pages 5-6, a storage means used to set a flag/marker – preferably one or two bits); and activating the selected hardware accelerator if the bit is set (Potts, col. 5, line 63 to col. 6, line 7).

As per claim 3, the combined system further teaches designating at least one register (Potts, col. 5, lines 50-62) within the register file to receive control commands from the plurality of processing elements; and activating the selected hardware accelerator to perform a media processing function according to a control command detected within the register (Lewis, page 5, bottom to page 6, line 10).

As per claim 4, the combined system teaches providing a selection unit (Lewis, 13) coupled to the plurality of hardware elements; designating at least one register (Potts, col. 5, lines 50-62) within the register file to receive control commands from the plurality of processing elements; directing the selection unit to provide a processing element with access to a selected hardware element and directing the selecting hardware accelerator to perform a media processing function according to a received control command (Lewis, by the controller 12; see page 5, bottom to page 6, line 10).

As per claim 5, the combined system teaches identifying a processing element have written the control command (Lewis, such as, by a flag); determining, according to the control command, an input data stream for the selected hardware accelerator (page 6, lines 1-10); determining, according to the control command, an output data stream for the selected hardware accelerator (Lewis, page 6, lines 1-10 and page 6, last paragraph); directing the selecting hardware accelerator to perform a media processing function according to a received control command (Lewis, by the controller 12; see page 5, bottom to page 6, line 10); updating a control bit within a register file to indicate whether data is available for one or more data dependent processing elements (Lewis, pages 5-8); requiring the one or more data dependent processing elements to wait to

execute instructions until the data it needs to execute the instructions is available in one or more register (Lewis, based on priority; see pages 7, top to mid of page 8).

Claims 7-10 are similar in scope to claims 2-5, and thus are rejected under similar rationale.

Claims 12-17 also are similar in scope to claims 2-5, and thus are rejected under similar rationale.

Claims 18-20 further require the hardware accelerators comprise image, video and audio processing hardware accelerators (Lewis, page 9, at the bottom and Potts, col. 4, line65, audio codec).

Claims 22-26 also are similar in scope to claims 2-5, and thus are rejected under similar rationale.

As per claims 28 and 29 (renumber as 27 and 28), the combined system fails to explicitly teach or suggest the RAM is a SDRAM and/or DDRSDRAM. It would have been obvious to one of ordinary skill in the art at the time the present invention was made to replace one type of RAM to another type of RAM is considered within the level of ordinary skill in the art based on the system requirement, for example, some want speed (fast) over cost (more expensive for fast memory).

Response to Arguments

6. Applicant's arguments with respect to claims 1-28 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kee M. Tung whose telephone number is 571-272-7794. The examiner can normally be reached on Tuesday - Friday from 5:30 am - 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ulka Chauhan can be reached on 571-272-7782. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kee M Tung
Primary Examiner
Art Unit 2671